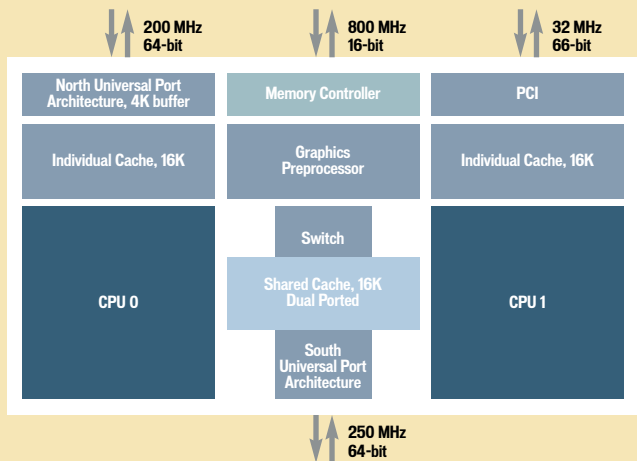


# Two Takes on CMP

Multiprocessor chip designers are taking different approaches to keeping CPUs fed with data. The Sun MAJC-5200 (left) will rely on two sets of 16KB cache reserves and multithreading to keep data flowing efficiently. IBM eschews multithreading in its Power4 design (right) but will pack the module with a second-level cache for chip-to-chip communications and a third-level cache to buffer information retrieved from system memory.

### Sun Microsystems' MAJC-5200



### IBM's Power4 Design

